Design of an event-driven random-access-windowing CCD-based camera

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Camera Objectives

- Adaptive sensor for real-time autonomous acquisition and tracking
- Sensor and control philosophy provides for inter-frame and intra-frame adaptation
- Sensor adjusts to dynamic target characteristics and environmental conditions
- Random-Access, Real-time Event-driven (RARE) camera

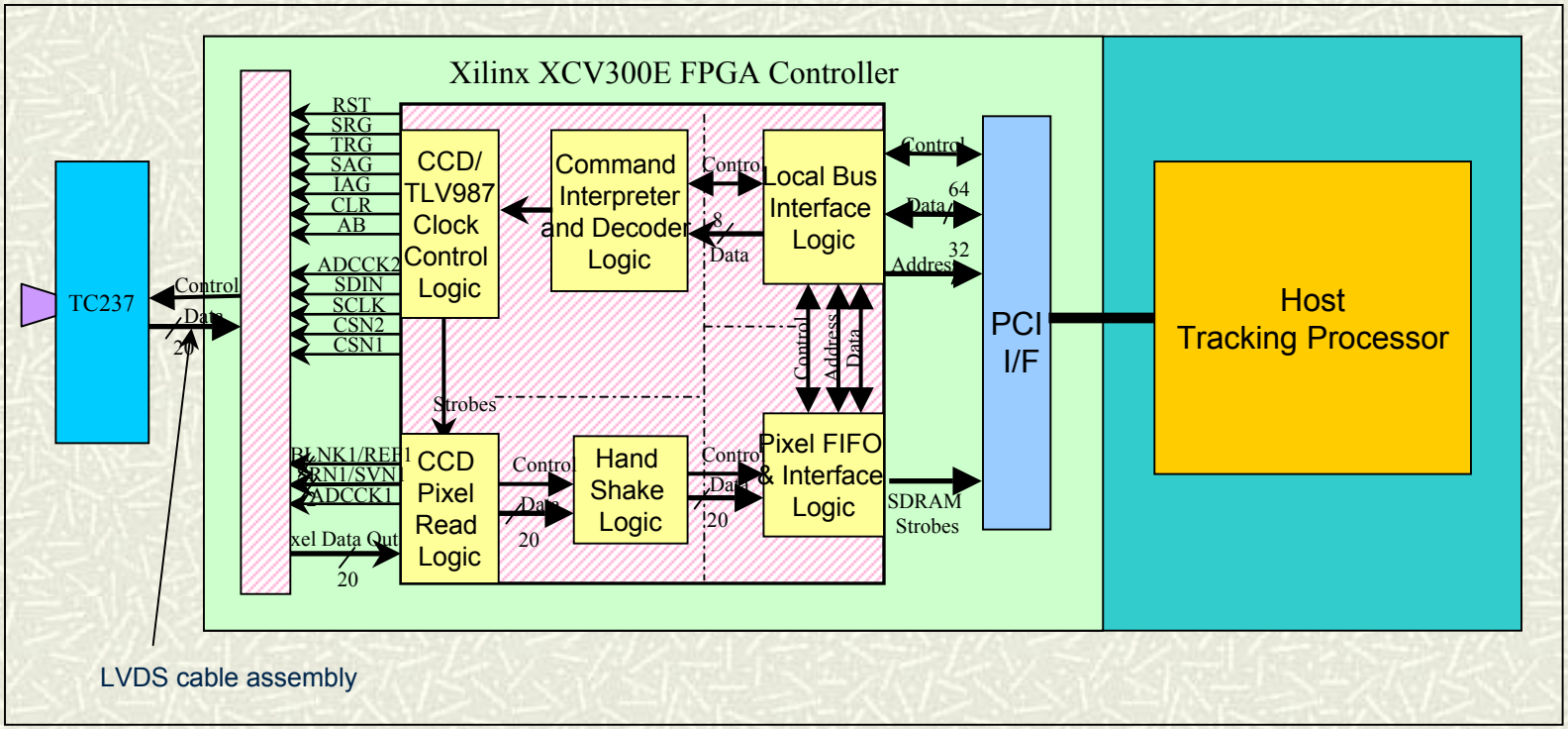
RARE Camera Version Definitions

	Camera v1.0	Camera v2.0	Camera v3.0
Interfaces	I/O to PCI	I/O to PCI	I/O to PCI
Max Frame Size	256x256	Full Frame	Full Frame
Exposure Control	Via Frame Rate	User Programmable via Hardware	User Programmable via Hardware
Frame Rate Control	Software Time Base	*User Programmable via Hardware*	User Programmable via Hardware
Pixel Processor (987) Programmability	Required	Required	Required
Windowing	Software	*User Programmable via Hardware*	User Programmable via Hardware
DMA	No	*Yes*	Yes
OS	RTOS	RTOS/Windows	RTOS/Windows
Auto-gain	No	No	Yes
Time-tagging	No	No	Yes
Pixel outputs	One	*Two*	Two
Multiple Operating Modes	No	*Yes*	Yes
Large image buffer for data storage	No	No	Yes
Pulsed Time Based Output	No	No	Yes
Sequenced Commands	No	No	Yes
Preprocessing of pixel data	No	No	Yes

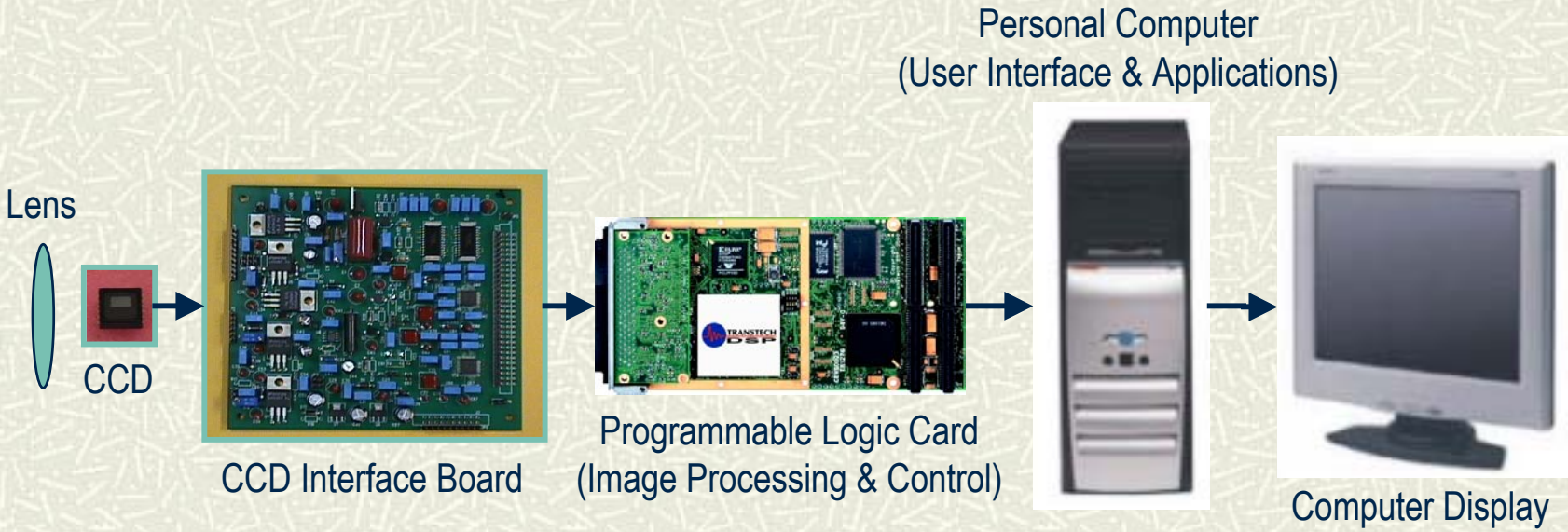
Hardware Components

- Custom CCD card
  - COTS Imager (TI 237B) 658 × 496
  - TI TLV987 signal processors
- LVDS cable for remote camera head configuration
- Commercial field programmable gate array (FPGA) card for low-level CCD control
  - TransTech PMCFPGA-01 card
  - 300K gate Xilinx XCV300E FPGA
- Host tracking processor
  - General-purpose computer with a 32-bit PCI bus
  - Provides FPGA control parameters
  - Reads camera status and pixel data

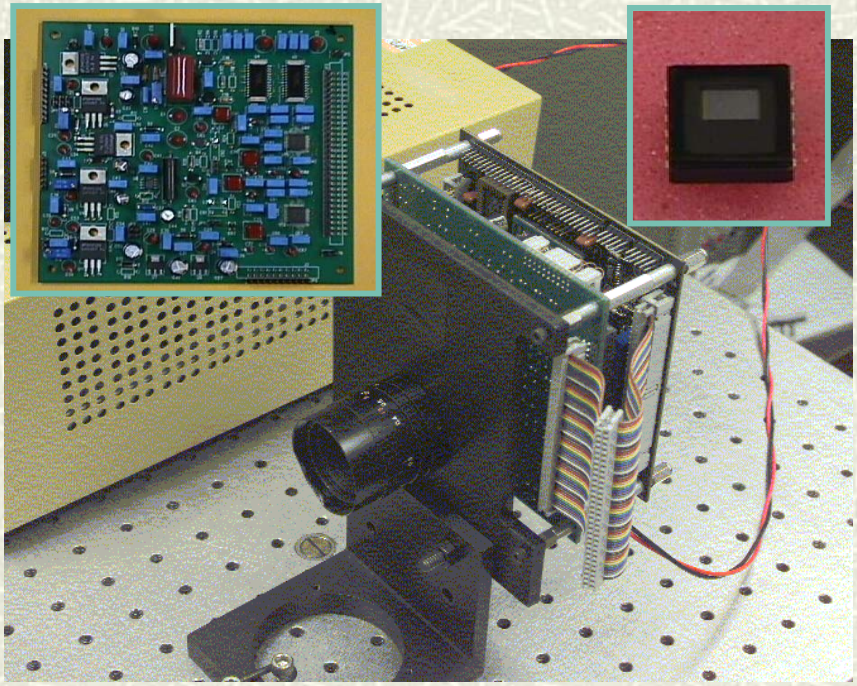
RARE Camera Architecture



System Hardware Block Diagram

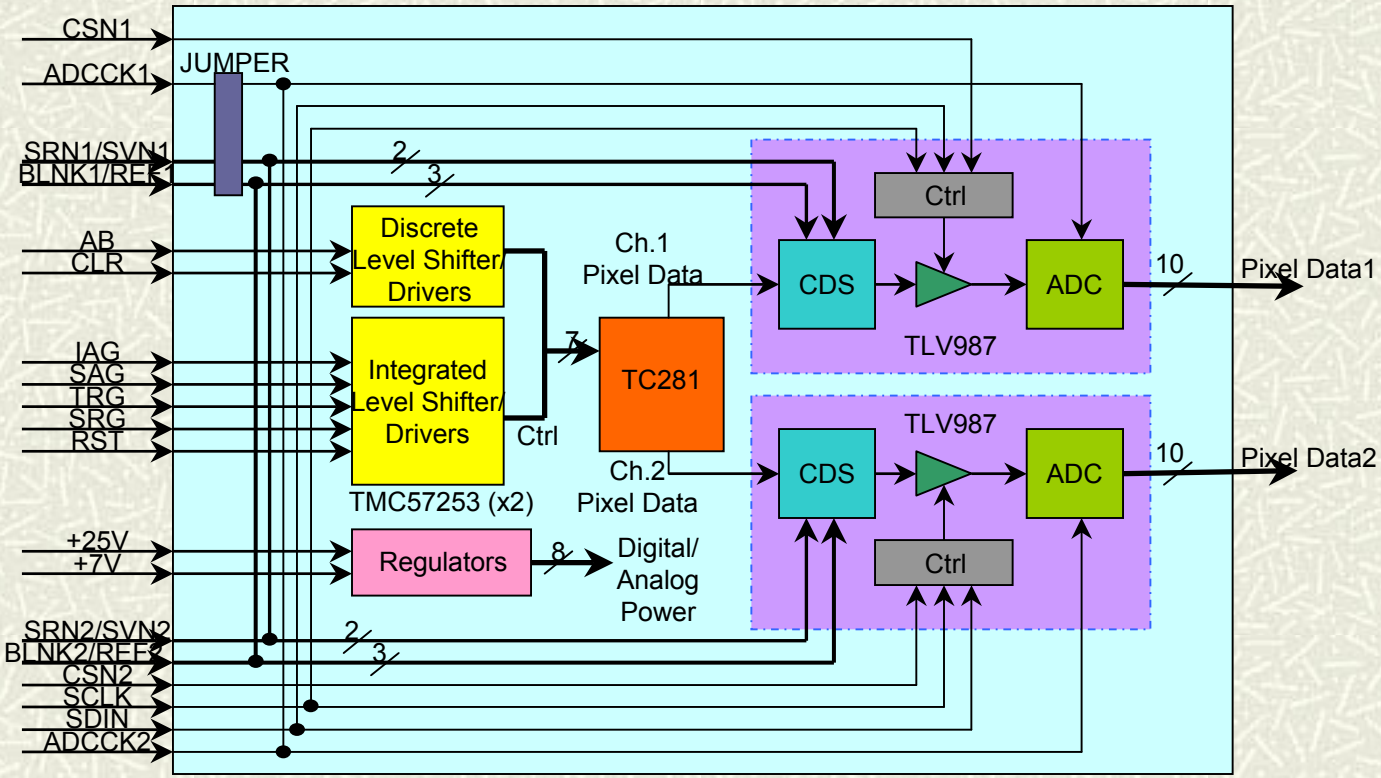


JPL CCD Card Assembly

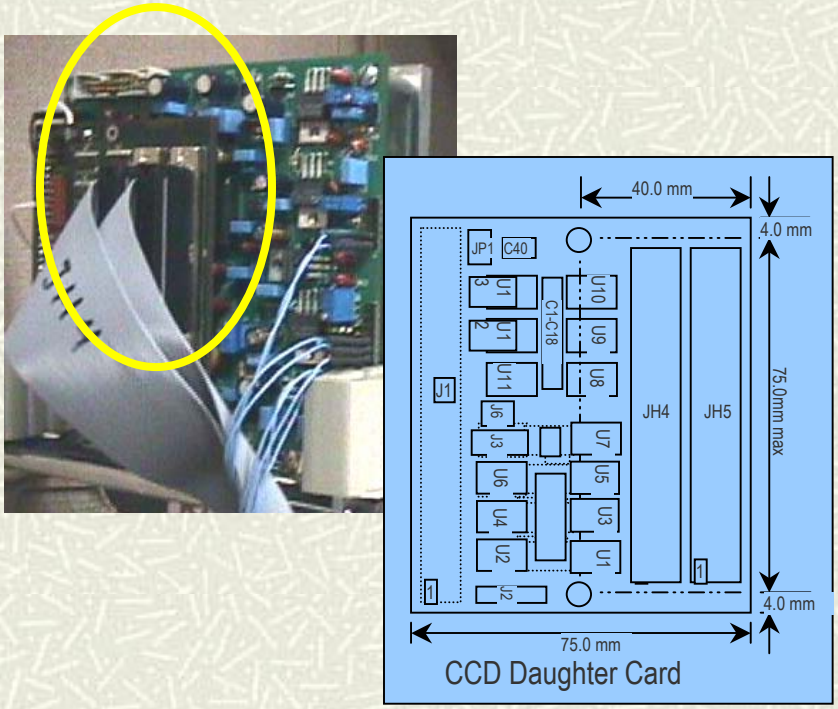


- Dynamic gain and bias control
- Digitized Video Output
- Region-of-Interest (ROI) Sub-Windowing Defined on Frame-by-Frame Basis
- 20 Mega pixel/second Readout Rate
  - 60 fps (658 × 496 pixels)
  - 800 fps (240 x 25 pixels)

CCD Card Block Diagram

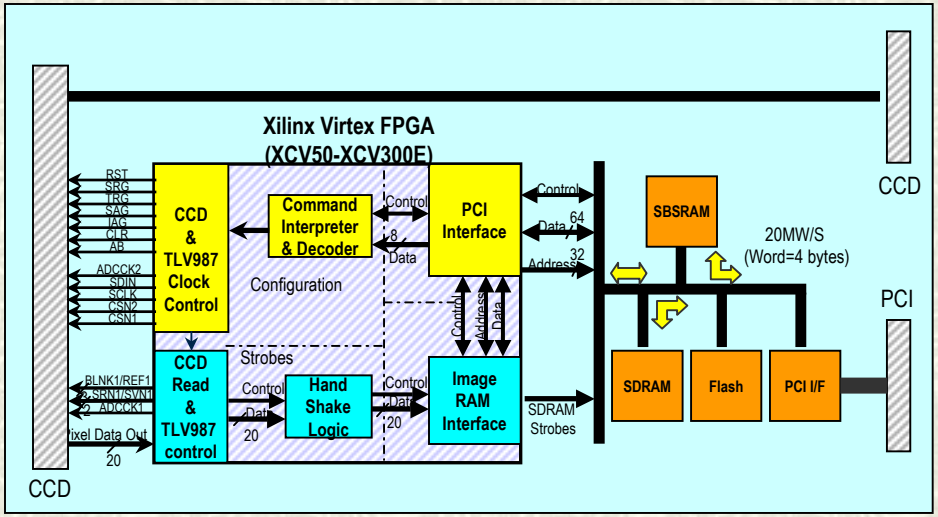


JPL Line Driver Daughter-Boards



- Allows CCD interface board to be separated from programmable logic control card by distances up to 10 m (remote camera head configuration)
- Supports maximum data rate from imager
- Digital link for noise immunity

Programmable Logic Card

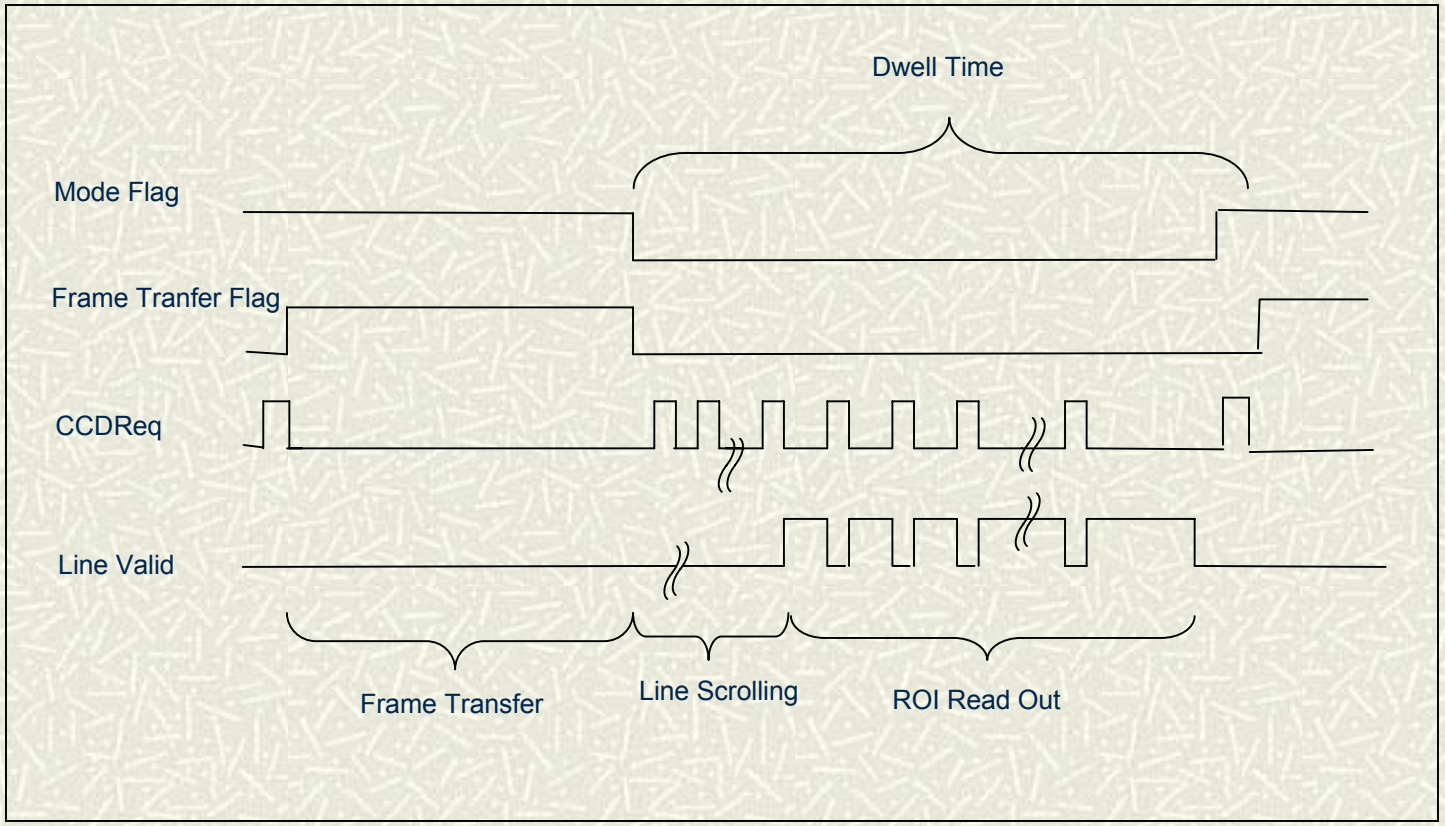


- FPGA firmware development platform
- PCI interface to host tracking processor
- Control for COTS CCD (658 × 496)
  - Region-of-interest (ROI) capability
  - Frame rate/integration time control

RARE Camera Registers

- Direct registers
  - Directly accessible via PCI bus
  - Define the FPGA configuration or initiate an action by the camera
- Buried registers
  - Accessed via camera commands
  - Used to modify group of functional registers
- TLV987 registers:
  - Accessed as buried registers
  - Control operation of signal processor chips

FPGA Controller Operation



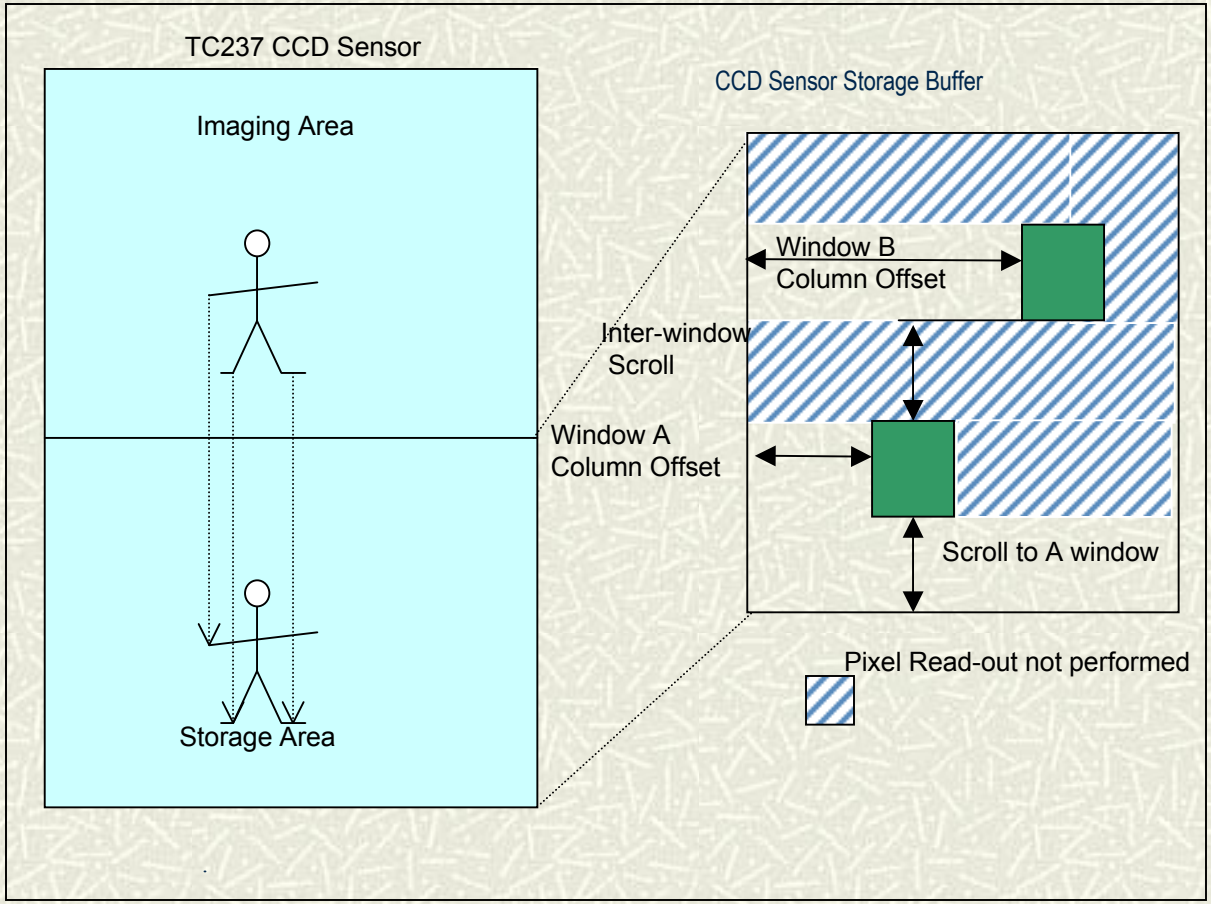
FPGA Controller Details

- Camera operation consists of
  - Frame transfer
  - Dwell time control
  - Line scrolling
  - ROI read out
- Frame transfer moves an image from the active image area to the CCD storage area
- Dwell time is the separation between frame transfers

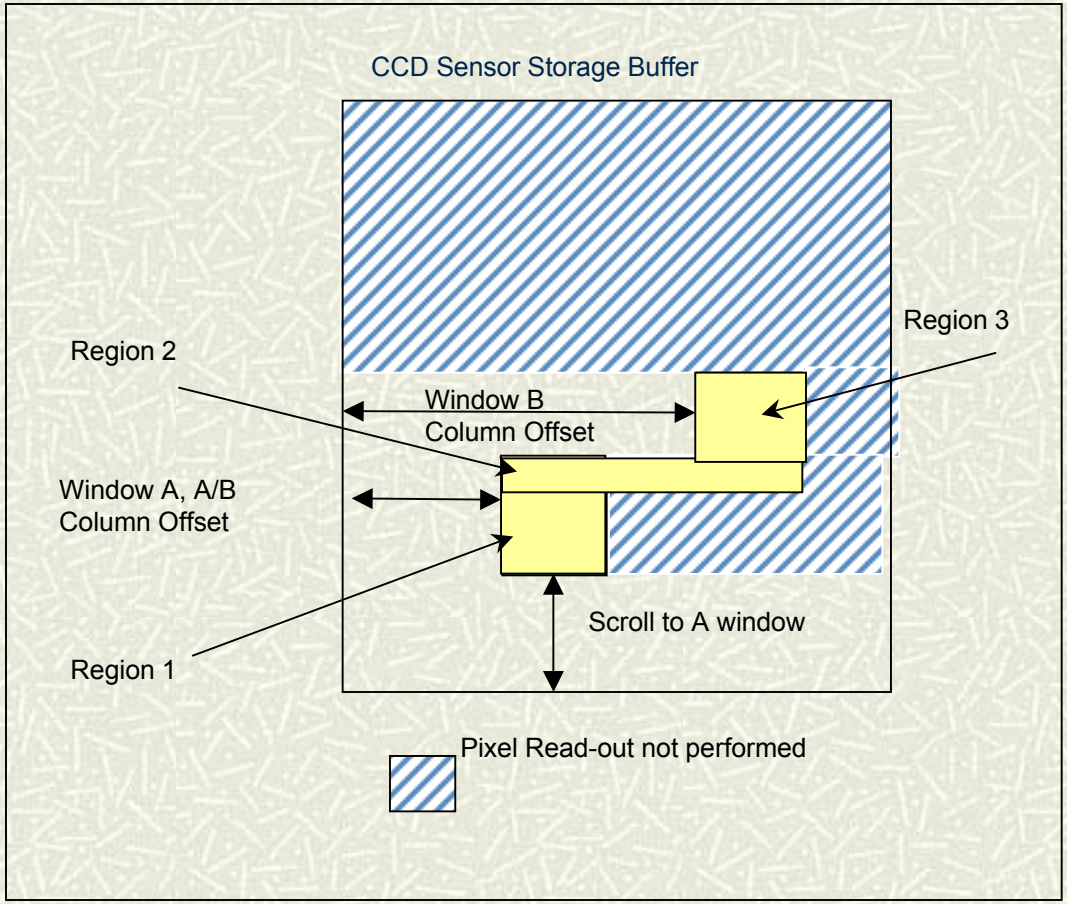
FPGA Controller Details (cont.)

- Frame transfer operating modes
  - Manual mode issues frame transfer when requested
  - Autonomous mode uses dwell time to request next frame transfer
- ROI read out
  - Defines ROI size and location parameters
  - Performs line scrolling as needed
  - Write pixels from the CCD storage area to the FPGA pixel FIFO

Frame Transfer and ROI read out



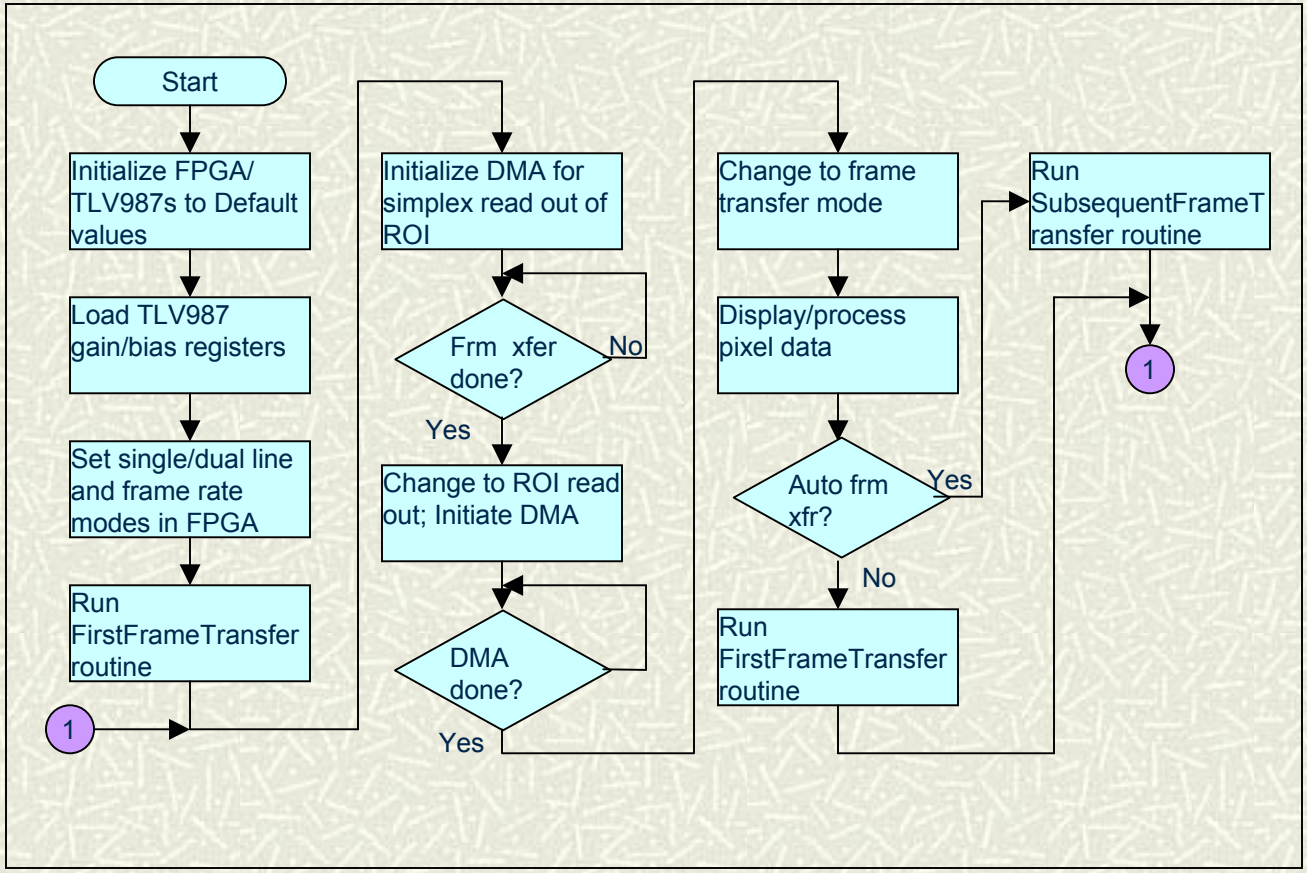
ROI Read Out with Common Rows



Host Tracking Processor Interface

- Host tracking processor communication
  - Via PCI bus
  - Single read/write access for control and status
  - Direct memory access (DMA) for pixel read out
- DMA operation
  - Defined by indivisible block transfer size with simplex or half-duplex operation
  - ROI read out operations use the simplex DMA mode
  - DMA operation is stalled at block boundaries for flow control

Tracking Processor Control Software



Benchmark Experiments

- Characterize actual frame rate for a single ROI per frame.
- Results show the achievable frame rates for different sizes and locations of ROIs within a frame.
- The maximum theoretical frame rates include
  - CCD frame transfer operation
  - ROI size and location definition
  - Pixel data transfer from the CCD to DMA memory in the host tracking processor
- Results do not include time needed to process or display the pixel data.

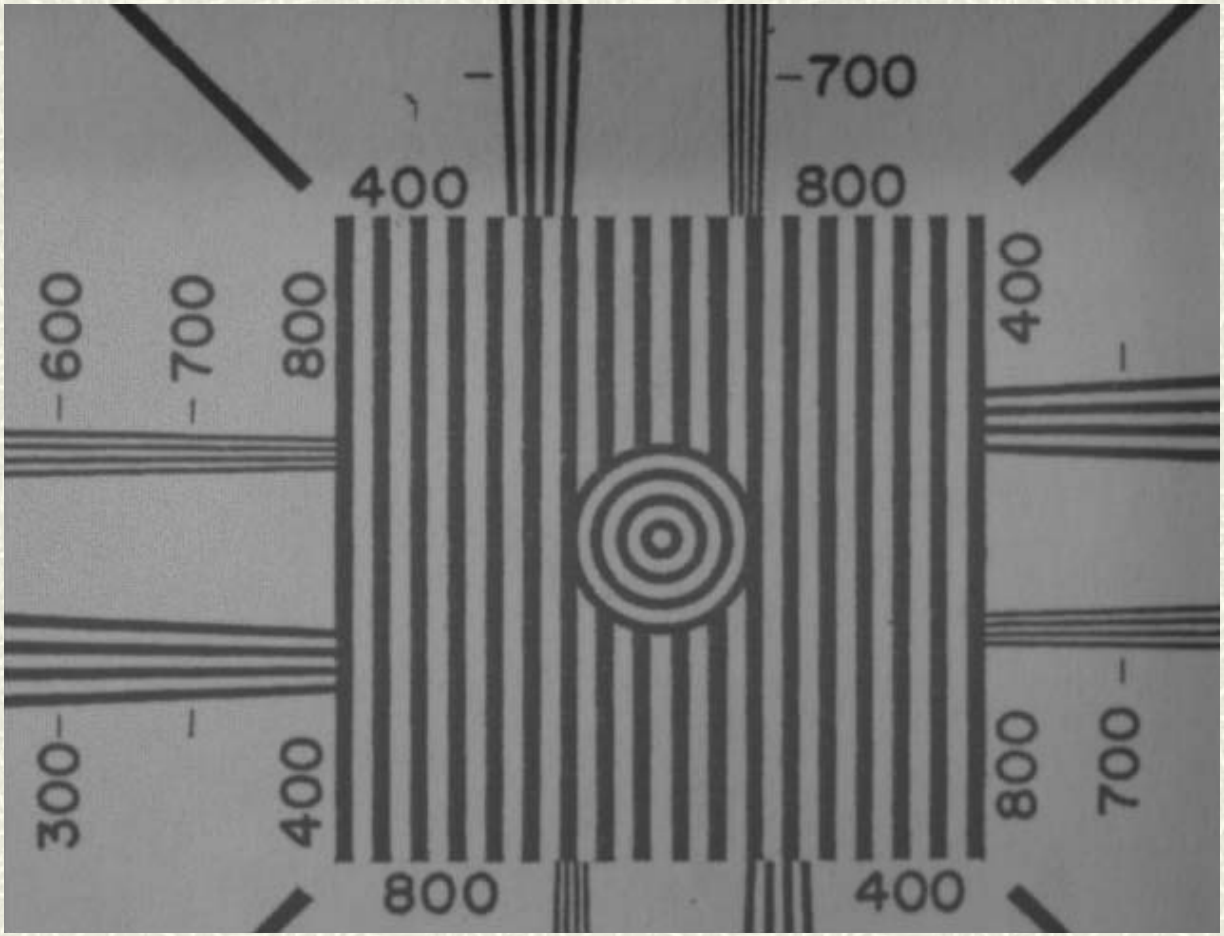
Experimental Set up

- Host tracking processor
  - IBM compatible PC
  - AMD 2000+ CPU with 512m dram
  - Windows 2000 operating system
- FPGA card
  - Commercial driver version pf_1.3r0 from Transtech
  - Custom firmware version pf1t_81v1b for local camera control
  - Manual frame transfer operation
- TC237 CCD card
  - Dual pixel stream operation
  - 10 mega pixels per second per stream

Experimental Set up (cont.)

- Pixel data read out uses DMA accesses
- Dwell and integration time are governed by the ROI read out time
- The frame transfer time for firmware version pf1t_81v1b is 100 micro seconds.

JPL CCD Assy. Image Data



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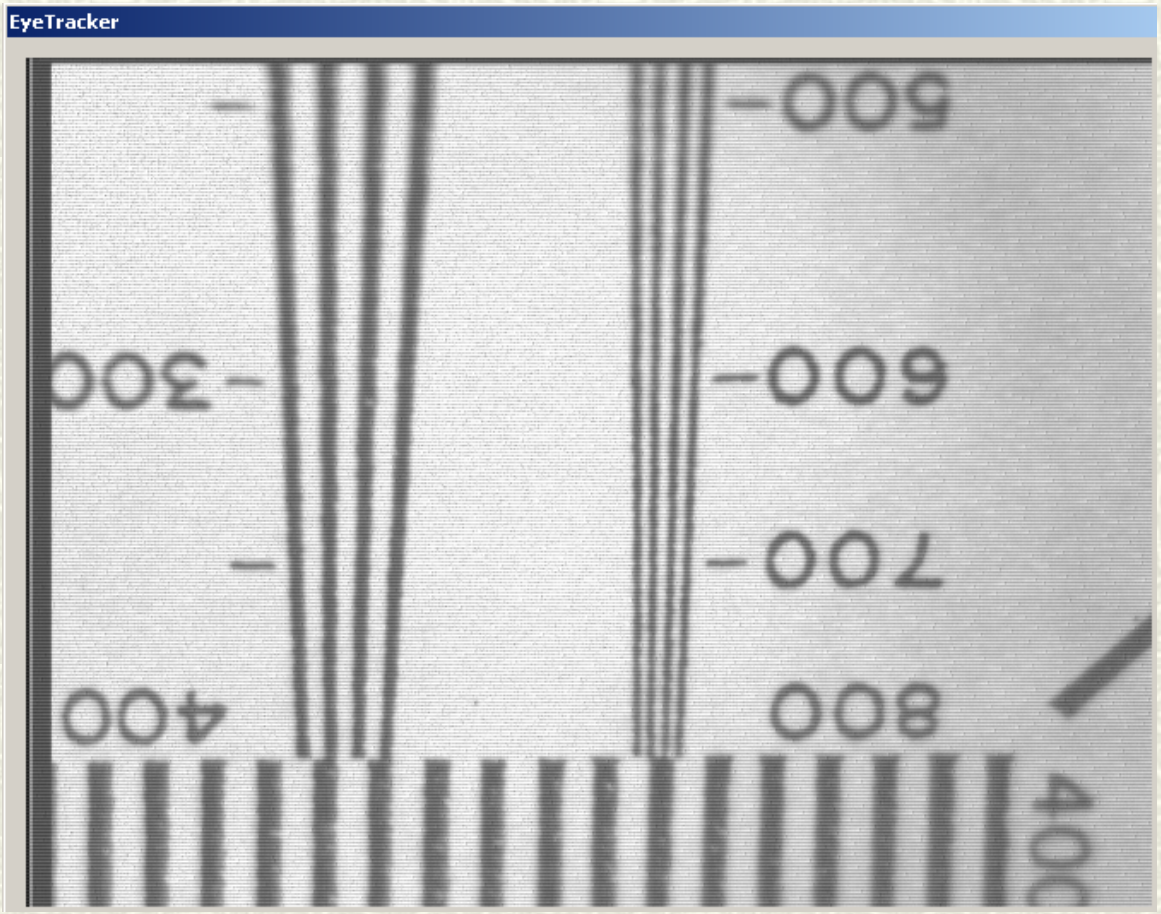
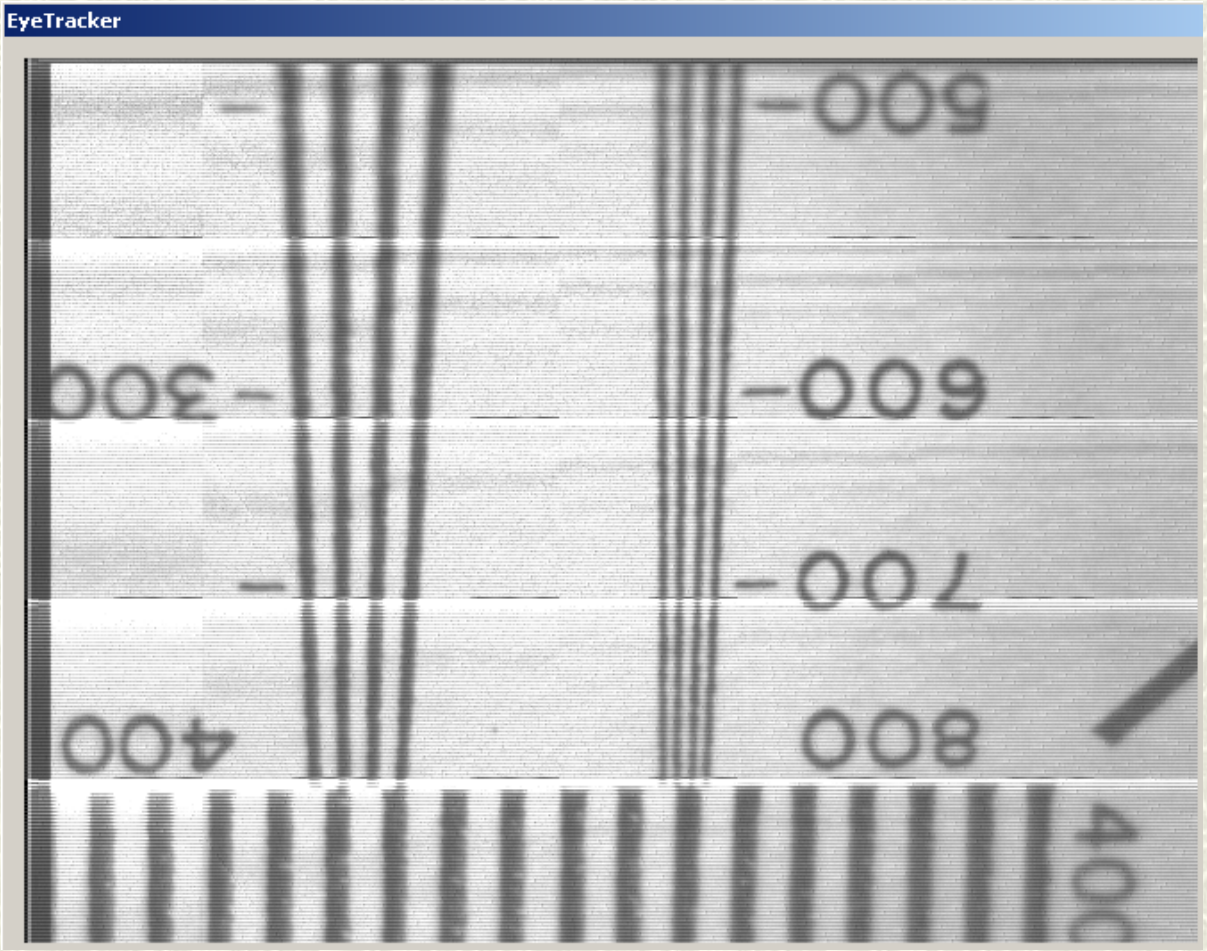
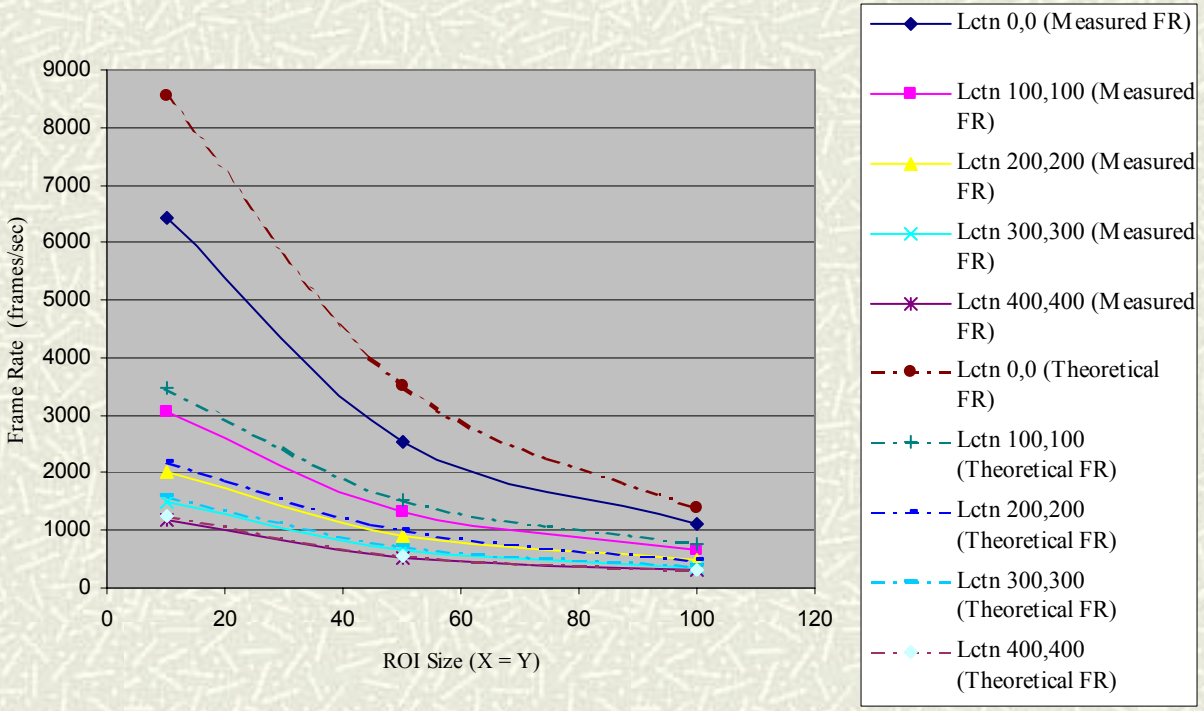


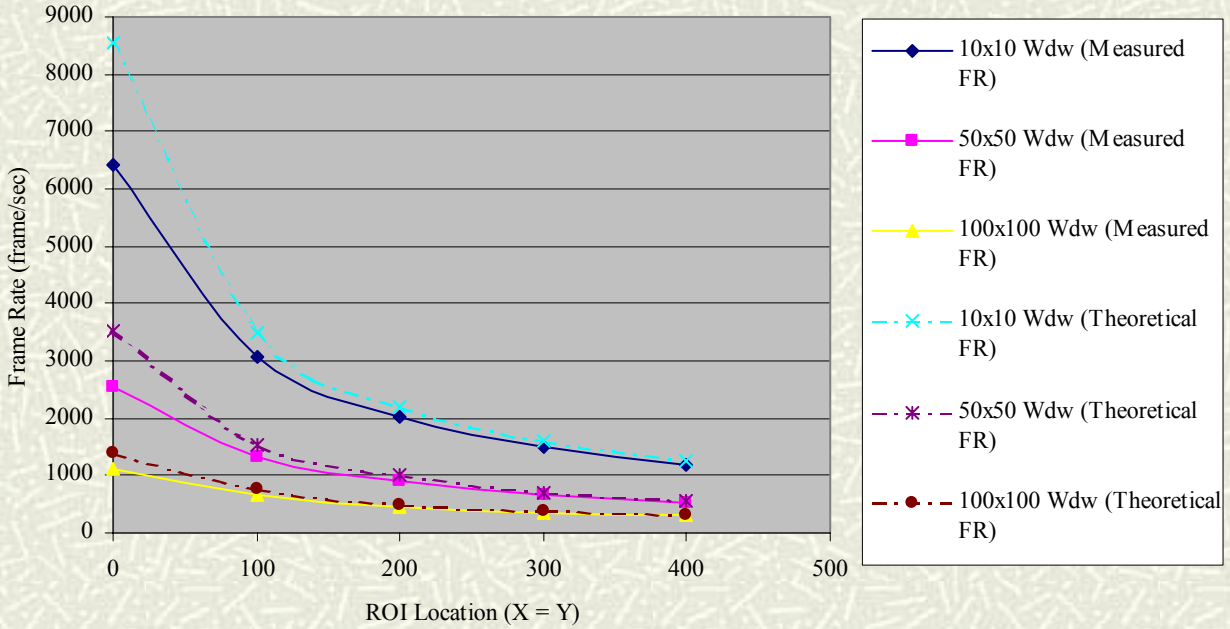
Tiled Image



Frame Rate vs. ROI Size Summary



Frame Rate vs. ROI Location Summary



Conclusions

- Developed a custom FPGA controller
  - Converts commercial CCD imager into a smart pixel device
  - Provides CCD control on a per-frame and intra-frame basis
  - Path to custom IC (ASIC) for integrated system
- FPGA controller and host tracking processor provide
  - Real-time event-driven imager control
  - Well suited to autonomous tracking applications
- Benchmark experiments achieved
  - 75% of the theoretical frame rates for this CCD imager
  - 6.4KHz for a10x10 ROI with origin at (0,0)
  - 1.1 KHz for a 10x10 ROI with origin at (400,400).